Questions pour Jon :

DDR :

• VTT does not terminate any DDR clock pairs. CK and CK# termination is a parallel 100–121Ω resistor between the two lines; Micron has found that only differential termination on CK and CK# produces optimal SI.

Terminaison de la DDR? Pour la ligne de clock.

• VTT islands require at least two additional decoupling capacitors (4–7µF) and two bulk capacitors (100µF) at each end.

Est-ce que les capacitors du TPS51200 sont assez gros? Ou il faut rajouter des plus bulk?

VTT must come after VDD

* VTT transient current can be as high as ±3.5A during heavy activity on the DQ and address buses. This transient current averages 0A, but can be somewhat random in nature, depending upon address/data patterns.

Je fais quoi de cet info là?